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Applicant:	Seidl, *et al.*	Docket No.:	INF-130
Serial No:	10/765,052	Art Unit:	2812
Date Filed:	January 28, 2004		
Title:	Method of Fabricating an Oxide Collar for a Trench Capacitor		

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- Certification of Facsimile Transmission (1 page)
- Submission of Papers Cited in Background Section (1 page)
- Copy of 1st Page of U.S. Patent No. 6,342,277 B1 (1 page)
- Copy of One (1) Cited Reference (4 pages)

Respectfully submitted,

Kristin R. Hayes
Legal Assistant

Confirmation Respectfully Requested

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Seidl, *et al.*	Docket No.:	INF-130
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SUBMISSION OF PAPERS CITED IN BACKGROUND SECTION

Dear Sir:

Applicants provide herewith the first page of U.S. Patent No. 6,342,277 B1 and the article entitled "Mass-Productive Ultra-Low Temperature ALD SiO_2 Process for Promising for Sub-90nm Memory and Logic Devices," to Park et al., (IEDM 2002), that are cited in the above-referenced application. Since the patent and article are not material to the patentability of any of the claims, Applicants believe that examination of these references is not necessary. However, since they were cited in the background, Applicants request that a copy of each be placed in the file.

Respectfully submitted,

January 24, 2006
Date

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Mass-Productive Ultra-Low Temperature ALD SiO_2 Process Promising for Sub-90nm Memory and Logic Devices

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Abstract

For the first time, ultra-low temperature ALD SiO_2 is successfully developed and applied on W/WN/poly-Si stack gate as a dual spacer for the enhancement of data retention time. ALD SiO_2 deposition is performed at 75℃ using HCD and H_2O as precursors and pyridine as a catalyst. Using ALD SiO_2 process, SiO_2 layer is deposited on W/WN/poly-Si stack gate without W oxidation. The gate resistances of W/WN/poly-Si stack gate do not exhibit any difference between SiN single spacer and SiO_2/SiN dual spacer schemes, which indicates that W oxidation does not occur during the ALD SiO_2 deposition for the formation of dual spacer. Conclusively, the significant improvement(>50%) of data retention time is achieved by employing SiO_2/SiN dual spacer at W/WN/poly-Si stack gate in 130nm DRAM device. In addition, excellent short channel characteristics of Vth is identified by applying low temperature ALD SiO_2 layer as a dual spacer on sub-100nm SRAM device.

Introduction

As the minimum feature size of DRAM is decreased below 100nm, W/WN/poly-Si stack gate should be adopted to reduce the word line resistance and the gate stack height at the same time.[1] In WSix gate, it is known that SiO_2/SiN dual spacer scheme results in better data retention characteristics in DRAM. The improvement of data retention time using dual spacer is mainly due to the minimization of dry etch damage during SiN spacer formation. W/WN/poly-Si stack gate, however, can not employ the dual spacer scheme due to the severe oxidation of W during high temperature CVD (HT-CVD) oxide deposition. In this study, we successfully developed atomic layer deposition(ALD) technique for SiO_2 deposition at low temperature. Furthermore, we firstly applied ALD SiO_2 layer on W/WN/poly-Si stack gate as a dual spacer without W oxidation and analyzed data retention characteristics as well as transistor characteristics.

Results and Discussions

1. Mass-Productive ALD SiO_2 Process

Fig. 1 shows the gas flow sequence of ALD SiO_2 process based on pyridine catalyzed $SiCl_4$(TCS) + H_2O → SiO_2 + HCl reaction.[2,3] The pyridine catalyst remarkably lowers a deposition temperature from >600K to room temperature. In our study, however, it is found that TCS based ALD SiO_2 process is not very satisfactory for device application due to low throughput and poor SiO_2 film quality. To overcome the drawbacks of TCS based ALD SiO_2 process, we firstly examined Si_2Cl_6(HCD) as a silicon precursor instead of TCS. In fact, HCD precursor shows a superior deposition rate as compared to TCS precursor.(Fig. 2) Furthermore, HCD based ALD SiO_2 film exhibits higher wet etch resistance than TCS based ALD SiO_2 film.(Fig. 3) Table 1 summarizes the basic properties of ALD SiO_2 process with HCD as a silicon precursor. The optimized process condition yields 1.5 Å/cycle deposition rate, <1% film uniformity, and excellent characteristics of process repeatability. The low level of film particle is also accomplished between in-situ chamber cleaning.

2. Properties of ALD SiO_2

Generally, SiO_2 film deposited at low temperature contains considerable amount of -OH group which degrades film properties. In this experiment, FT-IR and AES analyses are performed to evaluate the HCD based ALD SiO_2 film with post annealing. FT-IR and AES analyses shown in Fig. 4, 5 strongly suggest that HCD based ALD SiO_2 film is completely transformed to stoichiometric SiO_2 film after post annealing at 700℃

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for 1min. Moreover, it is confirmed that the impurity levels of C and Cl are below detection limit in AES spectra. As shown in Fig. 6, the deposited film thickness of ALD SiO_2 shows a good linearity with the number of process cycles. The surface RMS roughness measured by atomic force microscopy(AFM) indicates that ALD SiO_2 yields much smoother surface than HT-CVD oxide even at thicker film.(Fig. 7) In addition, ALD SiO_2 film exhibits the excellent step-coverage(over 95%) with no pattern loading effect.(Fig. 8). It is also confirmed that the electrical property of ALD SiO_2 evaluated by SIS capacitor structure is comparable with that of HT-CVD oxide as shown in Fig. 9.

3. ALD SiO_2 as a Dual Spacer at Metal Gate in DRAM

In general, dry etch damage induces defect-assisted junction leakage current and results in poor characteristics of data retention time in DRAM cell. To minimize the dry etch damage during the spacer formation, oxide buffer layer is added as a etch stopping layer prior to SiN deposition.(Fig. 10) In fact, SiO_2/SiN dual spacer scheme has a strong advantage over SiN single spacer for the enhancement of data retention time. Fig. 11 shows vertical structures of W/WN/poly-Si stack gate covered by HT-CVD oxide and ALD SiO_2 for the formation of SiO_2/SiN dual spacer. As shown in Fig 11, W word line was severely oxidized during HT-CVD oxide process, while SiO_2/SiN dual spacer is successfully formed by ALD SiO_2 process. In Fig. 12, the word line resistance of 176K cell array with ALD SiO_2/SiN dual spacer is identical to that with SiN single spacer, which strongly suggests no oxidation of W during the ALD SiO_2 process. Shown in Fig. 13 is the remain oxide thickness on S/D region in DRAM cell after SiN spacer etch back process. As expected, the sample with SiO_2/SiN dual spacer results in better controllability of thickness and thickness uniformity of remain oxide after SiN etch back. As a result, the single bit fail counts in Fig. 14, which is caused by poor data retention characteristics, are dramatically improved using ALD SiO_2/SiN dual spacer as compared to that of SiN single spacer. Fig. 15 shows single bit fail counts related to refresh time. The data retention time shows the substantial difference between dual spacer and single spacer schemes. In fact, more than 50% improvement of data retention time is achieved using ALD SiO_2/SiN dual spacer on W/WN/poly-Si stack gate. These superior characteristics of data retention time using dual spacer on metal gate are very promising for the fabrication of next generation high performance DRAM device.

4. Another Promising Application of ALD SiO_2

In high performance logic or SRAM devices, one of the most critical issues is the high thermal budget after channel and LDD implantations since it deteriorates short channel characteristics. The low temperature ALD SiO_2 layer is applied to poly-Si gate as a dual spacer on sub 100nm SRAM device. As shown in Fig 16, excellent short channel characteristics of Vth is identified by simply replacing HT-CVD oxide with ALD SiO_2 in dual spacer. Furthermore, drain induced barrier lowering(DIBL) characteristics in Fig. 17 are improved using ALD SiO_2 dual spacer. The overlap capacitance of ALD SiO_2 group is also smaller than that of HT-CVD oxide goup as shown in Fig. 18. Conclusively, low temperature ALD SiO_2 process can give a larger process window for the fabrication of sub 100nm high performance logic or SRAM devices.

Conclusion

For the first time, mass-productive ultra-low temperature ALD SiO_2 process is successfully developed using HCD and H_2O as precursors and pyridine as a catalyst. By applying ultra-low temperature ALD SiO_2 process for dual spacer, the significant improvement of data retention time is achieved at W/WN/poly-Si stack gate in 130nm DRAM device. It is also suggested that ALD SiO_2 process is very effective to retard SCE in CMOSFETs.

References

[1] S. Choi et. al., "Highly manufacturable Sub-100nm DRAM integrated with full functionality," 2002 Symp. of VLSI Tech., p54, 2002

[2] J. W. Klaus , et. al., "Atomic layer deposition of SiO_2 using catalyzed and uncatalyzed self-limiting surface reactions," Surface Review & Lett., 6, p435, 1999

[3] J. W. Klaus, et. al., "Growth of SiO_2 at room temperature with the use of catalyzed sequential half-reactions," Science, 278, p1934, 1997

Table I. Basic properties of ALD SiO_2 process

Deposition Rate	1.5 Å/cycle
Wet Etch Rate after 700℃, 1min. anneal	30 Å/min. in 200:1 HF
Particles >0.16㎛ size	<25 adders
Uniformity (1sigma)	< 1% within wafer
	< 1% in batch
	< 1% lot to lot

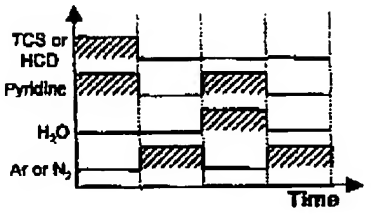

Fig. 1 Time sequence of Pyridine catalyzed ALD SiO_2 process

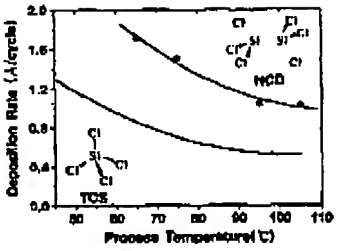

Fig. 2 Temperature dependence of deposition rate on different precursors

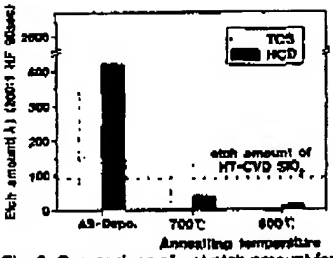

Fig. 3 Comparison of wet etch amount for HCD vs. TCS based ALD SiO_2 (As-deposition and post annealing temperature)

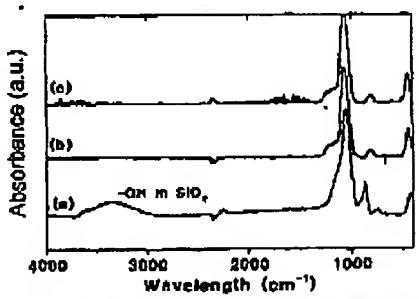

Fig. 4 FTIR spectra of (a) ALD SiO_2, as-deposition (b) ALD SiO_2 after annealing at 700°C, 1min. (c) HT-CVD SiO_2

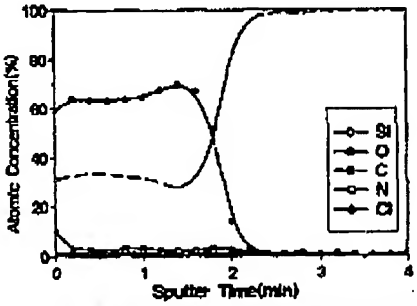

Fig. 5 AES depth profile spectra of ALD SiO_2

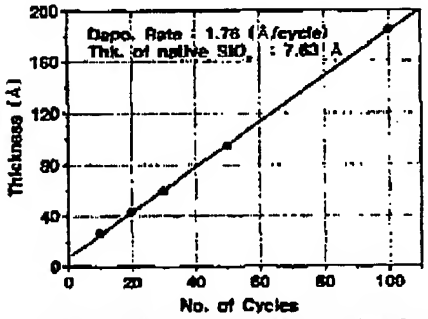

Fig. 6 ALD SiO_2 Thickness versus number of process cycles

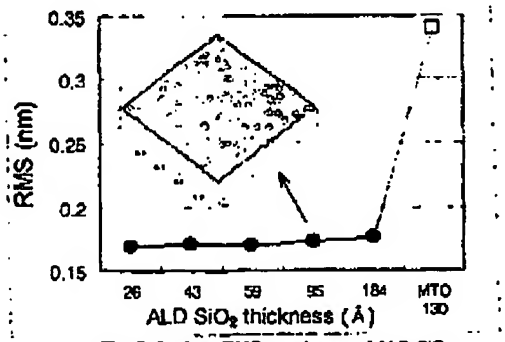

Fig. 7 Surface RMS roughness of ALD SiO_2 films measured by AFM

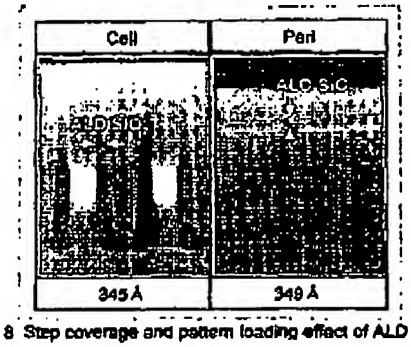

Fig. 8 Step coverage and pattern loading effect of ALD SiO_2

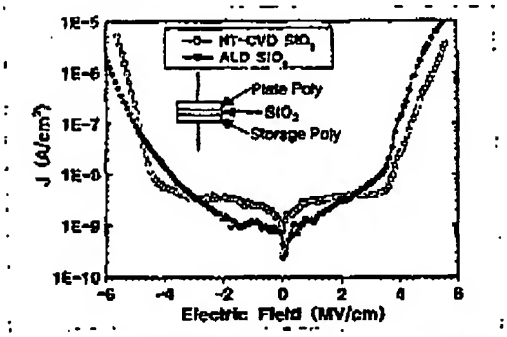

Fig. 9 J-E characteristics of ALD SiO_2 vs. HT-CVD SiO_2

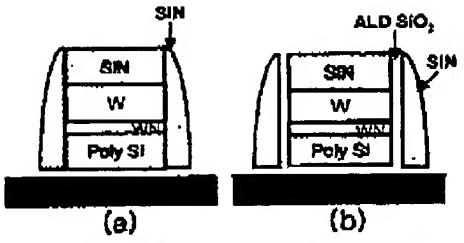

Fig. 10 Schematic diagrams of W/WN/poly-Si gate structure (a) SiN single spacer (b) SiO_2/SiN dual spacer

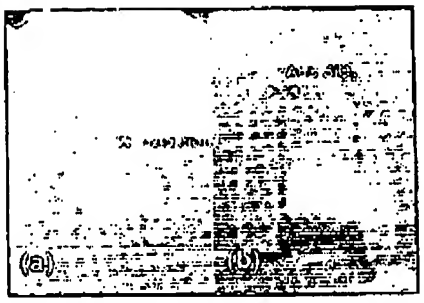

Fig. 11 Vertical SEM images of W/WN/poly-Si gate covered by SiO_2 layer for dual spacer (SiO_2/SiN). (a) HT-CVD SiO_2, (b) ALD SiO_2

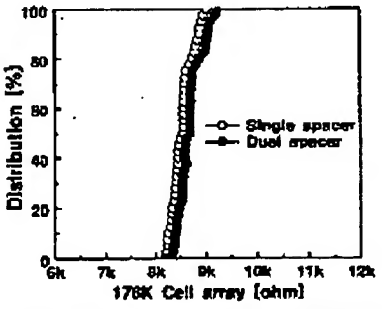

Fig. 12 Distribution of word line resistance in 176K cell array for different spacer schemes

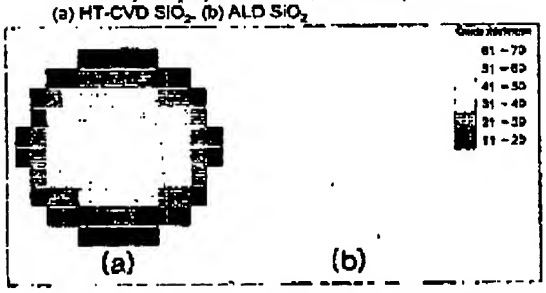

Fig. 13 Thickness of remain oxide at S/D region in DRAM cell (a) single spacer, (b) dual spacer

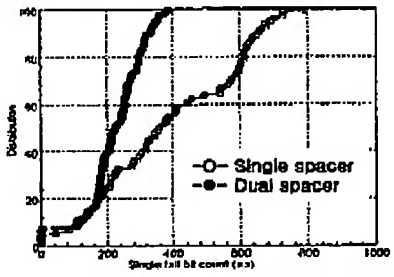

Fig. 14 Distribution of single bit fail counts for different spacer schemes

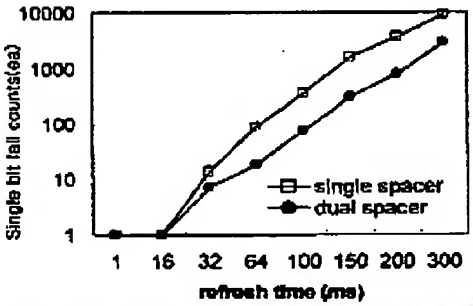

Fig. 15 Comparison of single bit fail counts for different spacer schemes

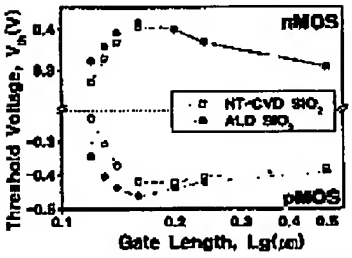

Fig. 16 ALD SiO_2 spacer shows better short channel characteristics due to lower thermal budget

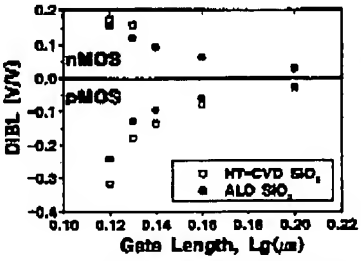

Fig. 17 Drain induced barrier lowering (DIBL) characteristics for two different oxides in dual spacer

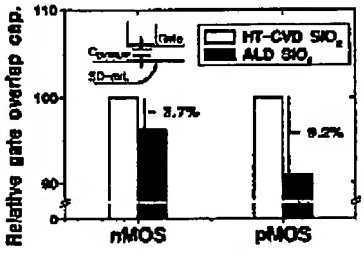

Fig. 18 Gate overlap capacitance : ALD SiO_2 vs. HT-CVD SiO_2 in dual spacer